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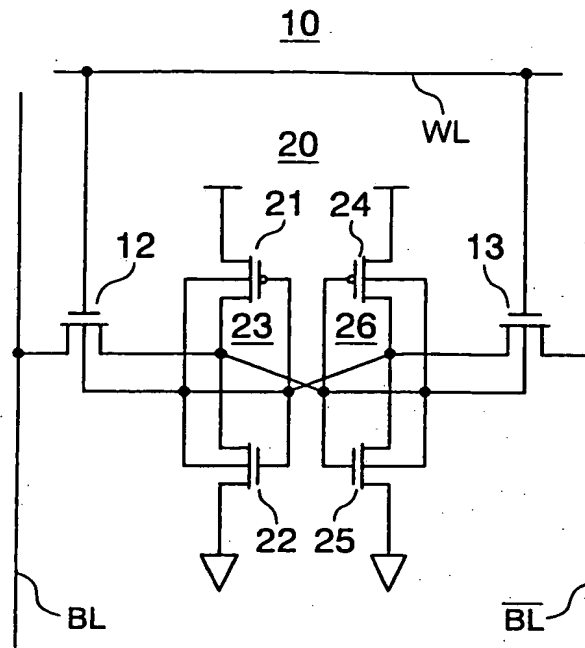


FIG. 1

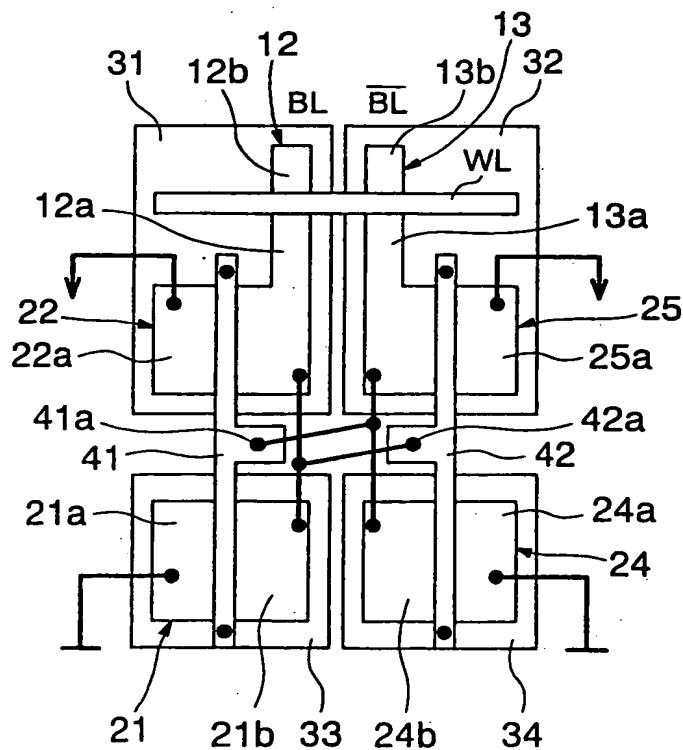
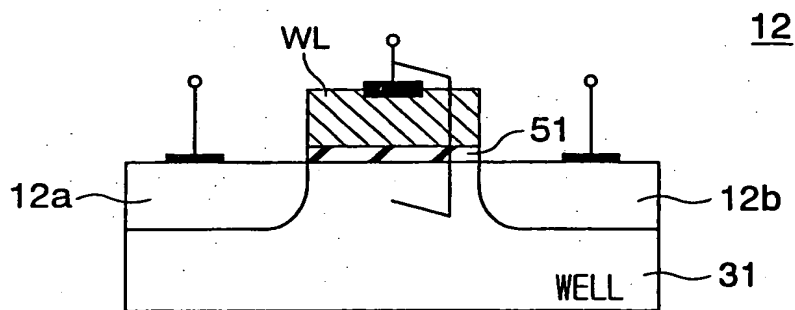


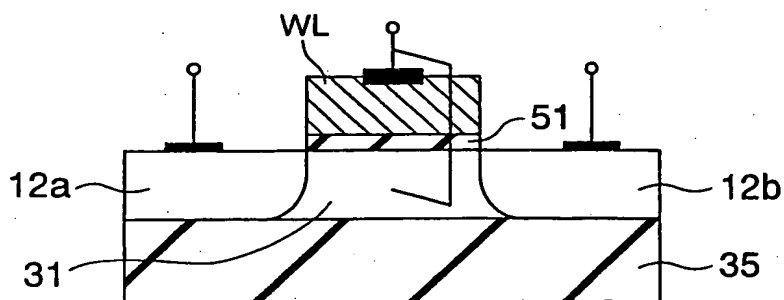
FIG. 2

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USE OF ORDINARY SEMICONDUCTOR SUBSTRATE

**FIG. 3A**



USE OF SOI SUBSTRATE

**FIG. 3B**

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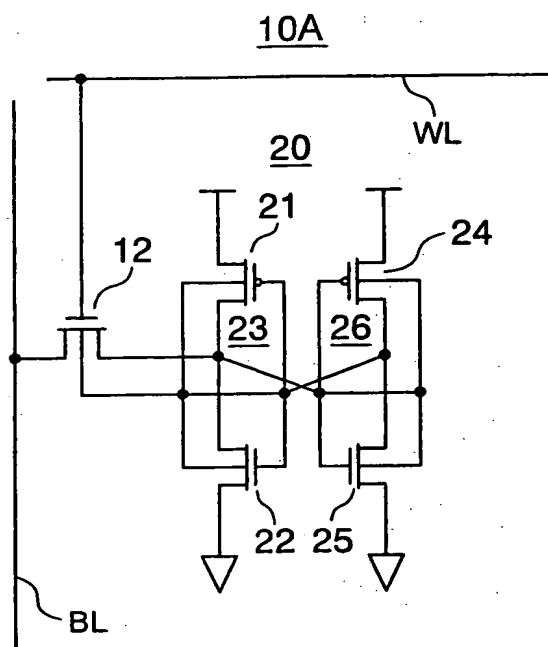


FIG. 4

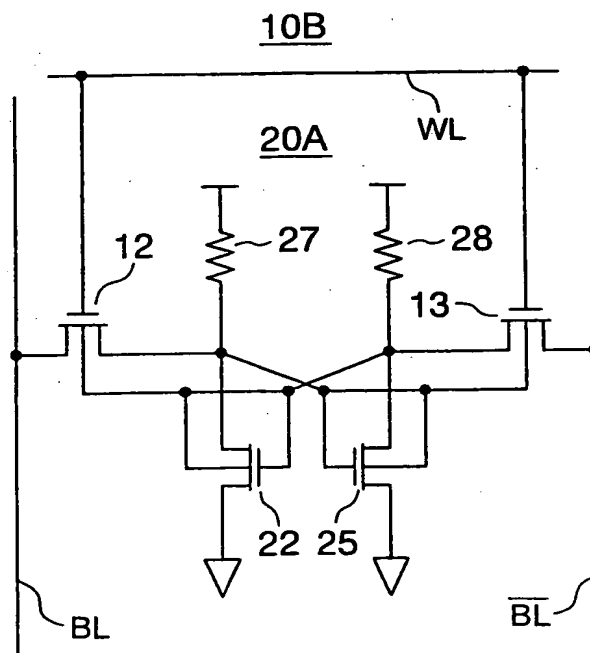


FIG. 5

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10C

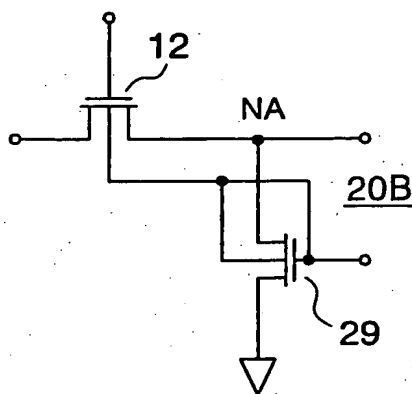


FIG. 6

10D

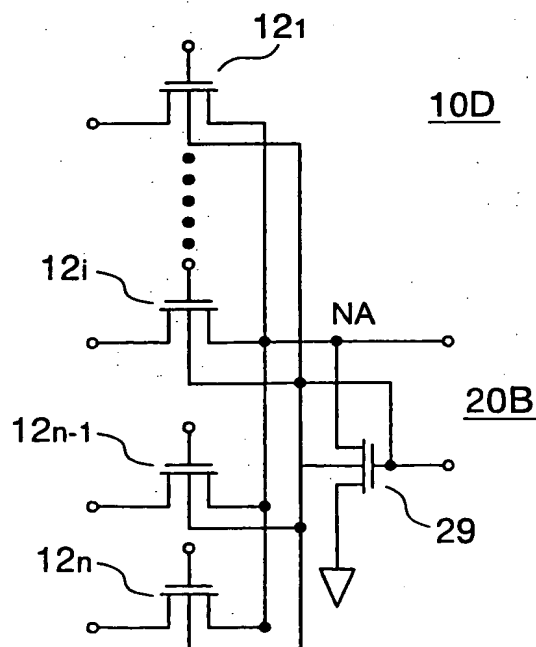
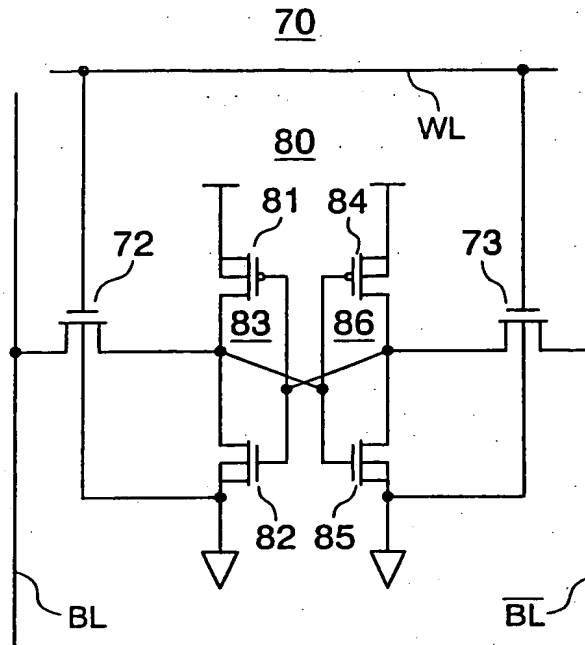
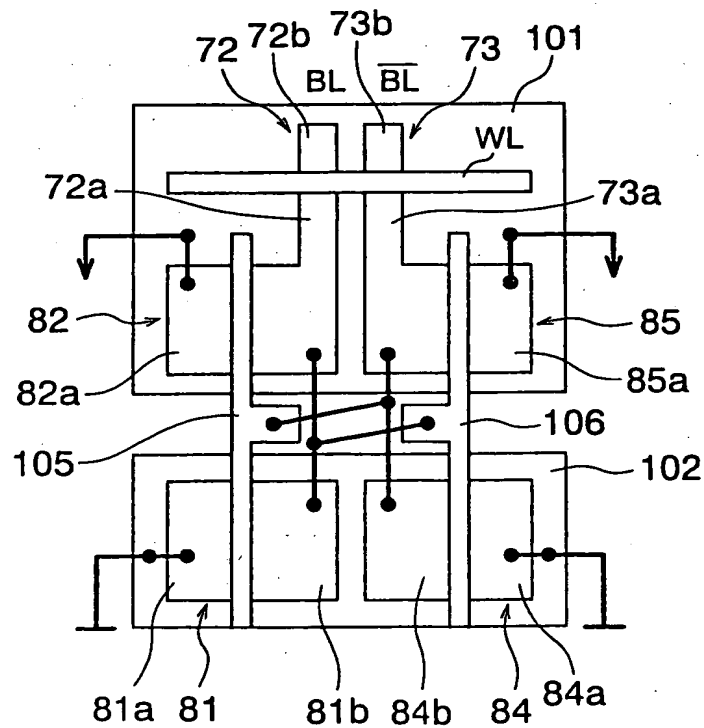


FIG. 7

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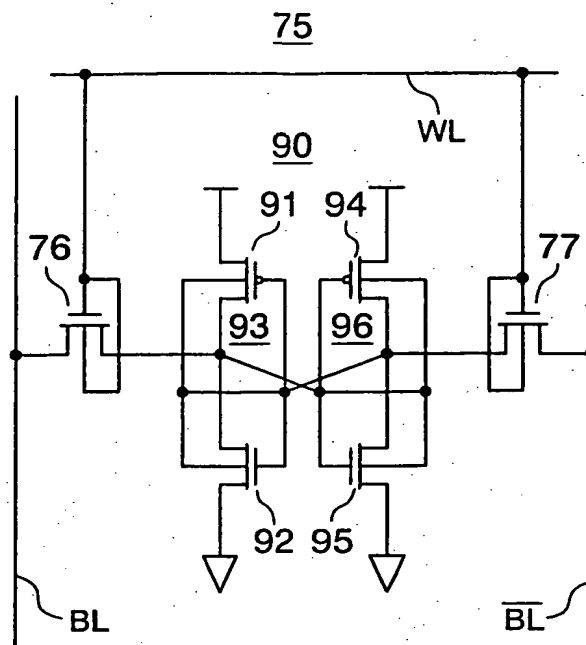


PRIOR ART  
FIG. 8

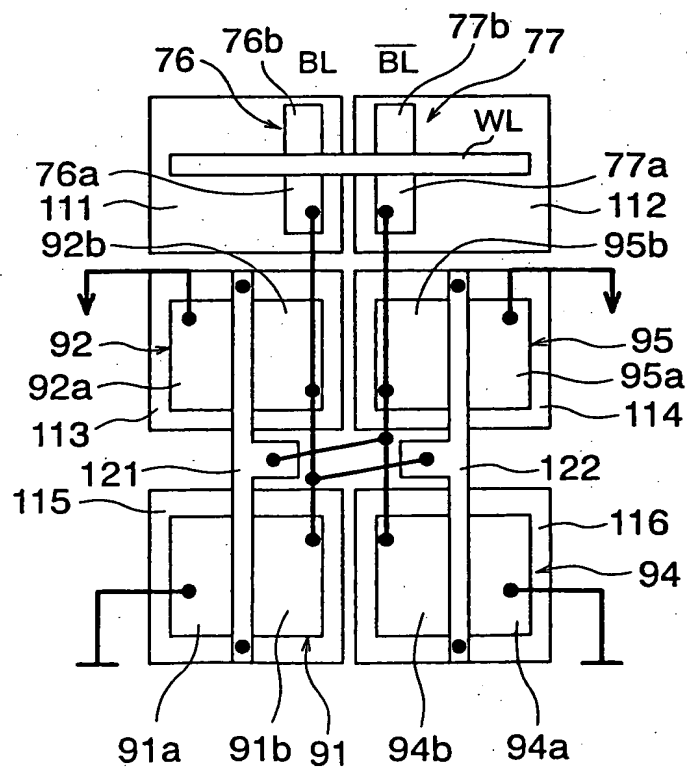


PRIOR ART  
FIG. 9

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PRIOR ART  
FIG. 10



PRIOR ART  
FIG. 11